

JEDEC STANDARD

Gunning Transceiver Logic (GTL) Low-Level, High Speed Interface Standard for Digital Integrated Circuits

JESD8-3A

(Revision of JESD8-3, November 1993)

MAY 2007

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS

(From JEDEC Board Ballots, JCB-93-11A and JCB-07-24, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc input and output specifications for a low-level, high-speed interface for integrated circuits.

1.1 Standard Specifications

Interface specifications for this standard are defined in Tables 1 and 2. Input specification requirements typically imply an input comparator stage operating about the specified reference voltage of 0.8 volt nominal. Output specifications include requirements for both an open-drain output stage requiring external termination and for an active-pullup, active-pulldown output stage that does not require external termination. In both cases the output high level is determined by a V_{TT} or V_{DDQ} voltage of 1.2 volts nominal.

1.1.1 Terminated Case

In the terminated case the output device is typically an open-drain MOS transistor. The output is returned to the V_{TT} termination voltage through a termination resistance.

1.1.2 Unterminated Case

In the unterminated case the output buffer has both an active-pullup and an active-pulldown transistor. For this case the nominal 1.2 volts is normally connected to a device pin (V_{DDQ}) to supply the upper level return for the pullup transistor such that, under no-load conditions, the output would typically pull to the V_{DDQ} voltage.

2 Application notes

2.1 Applicability to Alternative Voltage Level Systems

GTL-compatible devices are expected to be used in systems with several V_{DD} power supply voltages including $V_{DD} = 5$ volts, 3.3 volts and 2.X volts, thereby preserving a consistent interface level specification through many generations of devices and power supply standards. Signal pin interconnection with devices operating with other than GTL/ I/O standard specifications will require appropriate translation circuitry.

Table 1 — GTL* Standard DC Operating Specifications for Terminated Case

Symbol	Parameter	Test Condition	Min	Typical (2)	Max	Units
V_{TT}	Termination Voltage	-	1.14	1.2	1.26	V
$V_{REF}(1)$	Reference Voltage	-	$(2/3)V_{TT} - 2\%$	0.8	$(2/3)V_{TT} + 2\%$	V
V_{IH}	High-Level Input Voltage	-	$V_{REF} + 0.05$	0.83	-	V
V_{IL}	Low-Level Input Voltage	-	-	0.77	$V_{REF} - 0.05$	V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 40$ mA	-	0.2	0.4	V
I_O	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{TT}$ Output Off	-	-	± 10	μV
I_I	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{TT}$	-	-	± 5	μV

NOTE 1 V_{REF} may be generated on or off the chip, but must track the termination voltage V_{TT} . V_{REF} and/or V_{TT} may be device input pins.

NOTE 2 Except for V_{TT} and V_{REF} , the typical values are shown for information only; they are not a requirement.

* GTL has been patented under US Patent Number 5,023,488 dated June 11, 1991. The patent relates to CMOS drivers and receivers for low voltage swing and low power dissipation. The patent owner has agreed to license the patent under RAND terms as required by JEDEC.

2 Application notes (cont'd)

2.1 Applicability to Alternative Voltage Level Systems (cont'd)

Table 2 — GTL Standard DC Operating Specifications for Unterminated Case

Symbol	Parameter	Test Condition	Min	Nom	Max	Units
$V_{DDQ(1)}$	Output Buffer Supply Voltage	-	1.14	1.2	1.26	
$V_{REF(2)}$	Reference Voltage	-	$(2/3)V_{DDQ} - 2\%$	0.8	$(2/3)V_{DDQ} - 2\%$	V
V_{IH}	High-Level Input Voltage	-	$V_{REF} + 0.05$	-	-	V
V_{IL}	Low-Level Input Voltage	-	-	-	$V_{REF} - 0.05$	V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 4 \text{ mA}(3)$	-	-	0.4	V
$V_{OH(4)}$	High-Level Output Voltage	$I_{OH} = 4 \text{ mA}$	$V_{DDQ} - 0.4$	-	V_{DDQ}	V
I_O	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{DDQ}$ Output Off	-	-	± 10	μV
I_I	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DDQ}$	-	-	± 5	μV

NOTE 1 V_{DDQ} is connected to one or more pins on the device and used internally on the chip to set the output value of V_{OH} . V_{DDQ} may also be used external to the chip to set the value of the output pin bus when the output is in the high-Z off condition.

NOTE 2 V_{REF} may be generated on or off the chip but must track the V_{DDQ} voltage. V_{REF} may be a device input pin.

NOTE 3 This value of I_{OL} is a lower limit of this standard. Other values of I_{OL} above this value are acceptable and considered to be encompassed within this standard.

NOTE 4 At the test condition of I_{OH} , the V_{OH} value establishes the upper voltage level requirements of the output pull-up transistor. This test condition is not intended to establish operating noise margins. The output V_{OH} may approach the V_{DDQ} rail when the active output is unloaded.

Annex A (informative) Differences between JESD8-3A and JESD8-3

This table briefly describes most of the changes made to entries that appear in this standard, JESD8-3A, compared to its predecessor, JESD8-3 (November 1993). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description of change
2	Changed footnote from: GTL has been patented. The patent relates to CMOS drivers and receivers for low voltage swing and low power dissipation. There is a one-time only licensing fee of not more than \$10,000 required of semiconductor suppliers only. US Patent Number 5,023,488 dated June 11, 1991. To: GTL has been patented under US Patent Number 5,023,488 dated June 11, 1991. The patent relates to CMOS drivers and receivers for low voltage swing and low power dissipation. The patent owner has agreed to license the patent under RAND terms as required by JEDEC.
2	Table 1: Changed V_{IL} value for max. from: $V_{REF} + 0.05$ to $V_{REF} - 0.05$ per errata dated September 9, 1998, typographical error.
3	Table 2: Changed V_{IL} value for max. from: $V_{REF} + 0.05$ to $V_{REF} - 0.05$ per errata dated September 9, 1998, typographical error.



Standard Improvement Form

JESD8-3A

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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